What is claimed is:

1. A downlink beam frame signal processing system for a communication satellite, the processing system comprising:

a packet switch routing self addressed uplink data to a memory, the memory comprising at least a first and a second downlink beam hop location storage;

a power amplifier for amplifying a waveform based in part on the uplink data for transmission; and

a power gating circuit coupled to the power amplifier and including a power gate input responsive to a power gating signal to remove RF power from at least a portion of the waveform, thereby reducing DC power consumption of the power amplifier.

2. The processing system of claim 1, wherein the power gating signal is indicative of unavailability of uplink data in the memory.

3. The processing system of claim 2, wherein unavailability of uplink data comprises too little uplink data to fill a payload field in the waveform.

4. The processing system of claim 2, wherein unavailability of uplink data comprises the absence of uplink data in the memory.

5. The processing system of claim 2, wherein unavailability of uplink data comprises too little uplink data to fill at least two payload fields in the waveform.

6. The processing system of claim 2, wherein the power gating signal is indicative of a predetermined satellite power requirement.

7. The processing system of claim 6, wherein the power requirement comprises an eclipse power requirement.

8. The processing system of claim 2, wherein the power gating signal is indicative of a statistical multiplexed estimate of downlink utilization.

9. The processing system of claim 2, wherein the power gating signal is indicative of a desired

average first hop location queue depth formed in the memory.

10. A method for processing a downlink beam frame signal, the method comprising:

switching self addressed uplink data into at least one of a first and second downlink hop location storage area in a memory;

amplifying a frame signal based in part on the uplink data for transmission; and

prior to transmission, power gating at least a portion of the frame signal in response to a power gating signal.

11. The method of claim 10, wherein power gating comprises power gating at least a payload of the frame signal in response to too little uplink data in the memory to completely fill the payload in the frame signal.

12. The method of claim 10, wherein power gating comprises power gating at least a payload of the frame signal in response to too little uplink data in the

memory to fill the payload in the frame signal beyond a predetermined threshold.

13. The method of claim 10, wherein power gating comprises power gating at least a payload of the frame signal in response to too little uplink data in the memory to completely fill at least two payload fields in the frame signal.

14. The method of claim 10, wherein power gating comprises power gating at least a payload of the frame signal in response to satellite power requirements.

15. The method of claim 14, wherein power gating comprises power gating at least a payload of the frame signal in response to satellite eclipse power requirements.

16. The method of claim 10, wherein power gating comprises power gating at least a payload of the frame signal in response to a statistical multiplexed estimate of downlink utilization.

17. The processing system of claim 10, wherein power gating further comprises maintaining at least one synchronization field in the frame signal.

18. A downlink beam frame signal processing system for a communication satellite, the processing system comprising:

a packet switch routing self addressed uplink data to a memory, the memory comprising at least first and a second downlink beam hop location storage; and

a waveform generator coupled to the packet switch, the waveform generator comprising a modulator for producing a waveform to be transmitted and a power gating input for carrying a power gating signal for removing power from at least a portion of the waveform before transmission.

19. The processing system of claim 18, further comprising a filter coupled to a modulator output carrying the waveform.

20. The processing system of claim 19, wherein the waveform has frequency content removed in a passband region of the filter in response to the power gating signal.

21. The processing system of claim 19, wherein a first payload section of the waveform has frequency content removed in a passband region of the filter in response to the power gating signal.

22. The processing system of claim 21, wherein a second payload section of the waveform has frequency content remove in the passband region of the filter in response to the power gating signal.